PCT

WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 5 :
H01L 29/784, 27/088

A1

(11) International Publication Number: WO 93/21659

(43) International Publication Date: 28 October 1993 (28.10.93)

(21) International Application Number: PCT/GB93/00792

(22) International Filing Date: 15 April 1993 (15.04.93)

(30) Priority data:
9208324.5 15 April 1992 (15.04.92) GB

(71) Applicant *(for all designated States except US)*: BRITISH TECHNOLOGY GROUP LTD. [GB/GB]; 101 Newington Causeway, London SE1 6BU (GB).

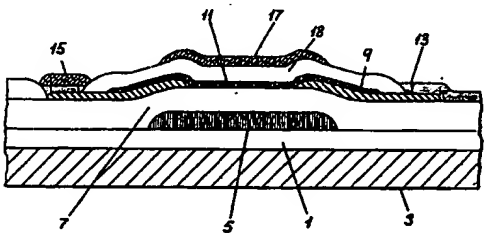
(72) Inventor; and
(75) Inventor/Applicant *(for US only)* : LEE, Michael, John [GB/GB]; 8 Lucas Road, High Wycombe, Buckinghamshire HP13 6QE (GB).

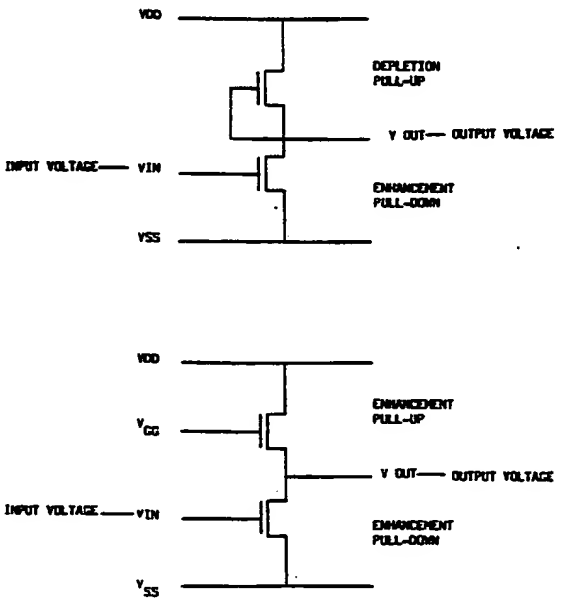
(74) Agent: CULLIS, Roger; Patents Department, British Technology Group Limited, 101 Newington Causeway, London SE1 6BU (GB).

(81) Designated States: JP, KR, US, European patent (AT, BE, CH, DE, DK, ES, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

Published
*With international search report.*

(54) Title: SEMICONDUCTOR DEVICES WITH A DOUBLE GATE




(57) Abstract

An integrated circuit arrangement comprising a pair of insulated-gate transistor devices connectible in series, the first transistor of said pair being operable as a depletion-mode device whilst the second transistor of said pair serves as an enhancement-mode device. A separately-biasable gate electrode permits the threshold voltage of the depletion-mode transistor to be adjusted independently.

*FOR THE PURPOSES OF INFORMATION ONLY*

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

| | | | | | |
|---|---|---|---|---|---|
| AT | Austria | FR | France | MR | Mauritania |
| AU | Australia | GA | Gabon | MW | Malawi |
| BB | Barbados | GB | United Kingdom | NL | Netherlands |
| BE | Belgium | GN | Guinea | NO | Norway |
| BF | Burkina Faso | GR | Greece | NZ | New Zealand |
| BG | Bulgaria | HU | Hungary | PL | Poland |
| BJ | Benin | IE | Ireland | PT | Portugal |
| BR | Brazil | IT | Italy | RO | Romania |
| CA | Canada | JP | Japan | RU | Russian Federation |
| CF | Central African Republic | KP | Democratic People's Republic of Korea | SD | Sudan |
| CG | Congo | | | SE | Sweden |
| CH | Switzerland | KR | Republic of Korea | SK | Slovak Republic |
| CI | Côte d'Ivoire | KZ | Kazakhstan | SN | Senegal |
| CM | Cameroon | LI | Liechtenstein | SU | Soviet Union |
| CS | Czechoslovakia | LK | Sri Lanka | TD | Chad |
| CZ | Czech Republic | LU | Luxembourg | TG | Togo |
| DE | Germany | MC | Monaco | UA | Ukraine |
| DK | Denmark | MG | Madagascar | US | United States of America |
| ES | Spain | ML | Mali | VN | Viet Nam |
| FI | Finland | MN | Mongolia | | |

# Semiconductor devices with a double gate

This invention relates to semiconductor devices and, in particular, to the fabrication of thin film transistors and integrated circuits incorporating such transistors.

In designing circuits for integrated electronics it is an advantage to have more than one type of active device available - for example CMOS has n and p channel and most n-MOS integrated circuit fabrication processes allow selective variation of threshold voltage and in particular fabrication of enhancement and depletion mode devices simultaneously. For an n-channel enhancement mode device the minimum current (off state) flows with zero applied gate voltage and is increased by applying a positive gate voltage (on state). Conversely for a depletion mode device a negative gate voltage is applied to turn the device off whilst at zero gate voltage the device is in the on state.

In n-MOS circuits use of enhancement-depletion circuitry gives improved performance when compared with enhancement-only circuits, in terms of switching speed, output voltage levels, and power consumption.

As indicated above, improved circuit performance is possible if depletion mode devices are also available. Possible ways to produce depletion type thin film active devices are to increase the semiconductor film thickness for the depletion devices as compared to the enhancement, or to selectively add n-type dopant material into the channel region of the depletion devices. In either case additional process steps would be needed, involving the use of extra mask layers, and hence increased cost and reduced yield. Depletion and enhancement devices may also be produced by using different geometries for the CdSe layers without an additional mask step.

We have devised a process using cadmium selenide which produces a double gated n-channel enhancement mode device, combining the desirable characteristics of high speed operation

due to the high carrier mobility, high on current and low off current.

It has been found possible to produce depletion-mode TFTs without any additional processing steps by biasing one of the gates of the device to control the threshold voltage of the device so that it has a suitable (negative) value. Thus the TFTs can be made to be enhancement or depletion types as required, with both types co-existing in the same circuit.

No alterations to the fabrication process are needed, and no additional mask layers, merely a small variation in mask design to allow separate control of the potential of both gates of the TFTs. An externally applied voltage is applied to one gate of the depletion mode devices in the circuit to set the required threshold voltage.

According to the present invention there is provided an integrated circuit arrangement comprising a pair of insulated-gate transistor devices connectible in series wherein the first transistor of said pair is operable as a depletion-mode device whilst the second transistor of said pair serves as an enhancement-mode device.

The invention will now be particularly described with reference to the accompanying drawings, in which:

Figure 1 is a cross-section through a thin film transistor in accordance with a specific embodiment of the invention;

Figure 2 shows electrical characteristics of the transistor of Figure 1; and

Figure 3 is the circuit diagram of an inverter; and

Figure 4 shows electrical characteristics of this inverter.

Referring now to the drawings, Figure 1 shows a cross-section through a thin film transistor in accordance with a specific embodiment of the present invention. A diffusion barrier 1 is formed on a substrate 3. The device has a bottom gate 5 separated by an insulator layer 7 from a layer of cadmium

selenide 9. An n-channel region 11 is formed in this semiconductor layer. A pad contact 13 and column conductor 15 are provide for the source and drain electrodes. An upper gate 17 is separated from the semiconductor by an insulator layer 19.

Figure 2 shows the current through the transistors as a function of the top gate voltage for two values of the bottom of the top gate voltage. It is seen there is a marked difference in the position of the curves particularly in the theshold region (i.e. the steeply rising part).

Figure 3. shows the circuit diagram of an inverter for use with the transistor of Figure 1. Its transfer characteristics are shown in Fig. 4. where the advantage of using the depletion TFT as the pull-up transistor is seen in the larger voltage swings. In the example chosen an enhancement pull-up device would not operate a shift register.

Fabrication of enhancement and depletion type CdSe thin film transistors is simultaneously possible, with no additional masking or processing steps to those required for a purely enhancement type process.

The same technique may be applied to the production of TFTs using other semiconductor materials. In the case of polysilicon this process would compensate for the low mobility of holes in p-type material and produce enhanced circuits.

Claims

1. An integrated circuit arrangement comprising a pair of insulated-gate transistor devices connectible in series characterised in that the first transistor of said pair is operable as a depletion-mode device whilst the second transistor of said pair serves as an enhancement-mode device.

2. An integrated circuit arrangement according to claim 1 characterised in that said first transistor of a separately-biasable gate electrode adapted to permit the threshold voltage of said transistor to be adjusted independently.

3. An integrated circuit arrangement according to claim 1 characterised in that the channel region of said transistors is formed of cadmium selenide.

4. An integrated circuit arrangement according to claim 1 characterised in that the channel region of said transistors is formed of silicon.

5. A switching circuit characterised in that it incorporates a pair of transistors in an integrated circuit arrangement in accordance with any one of the preceding claims.

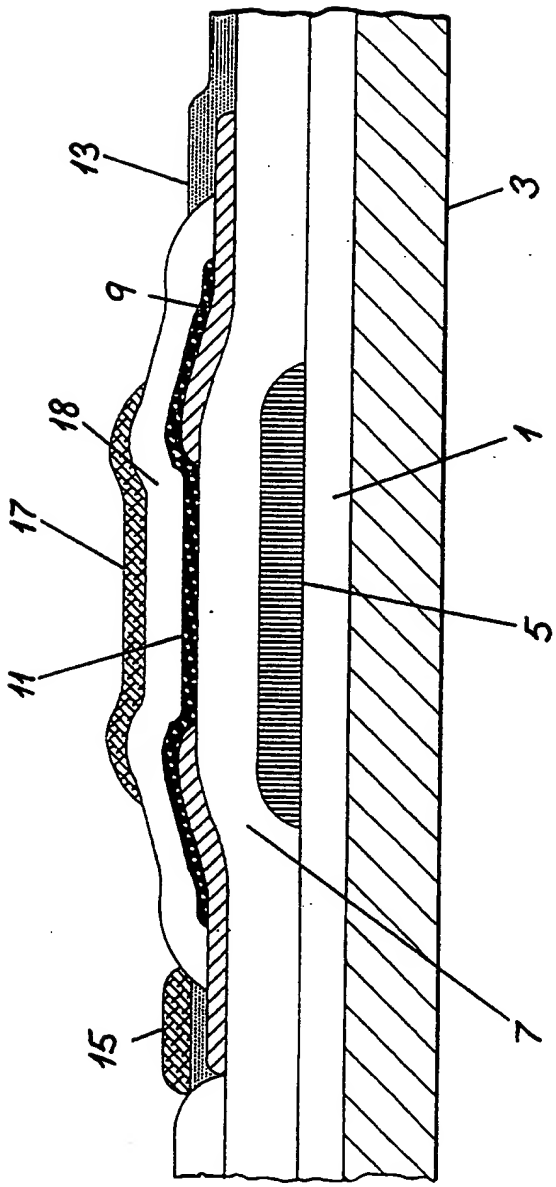



Fig. 1

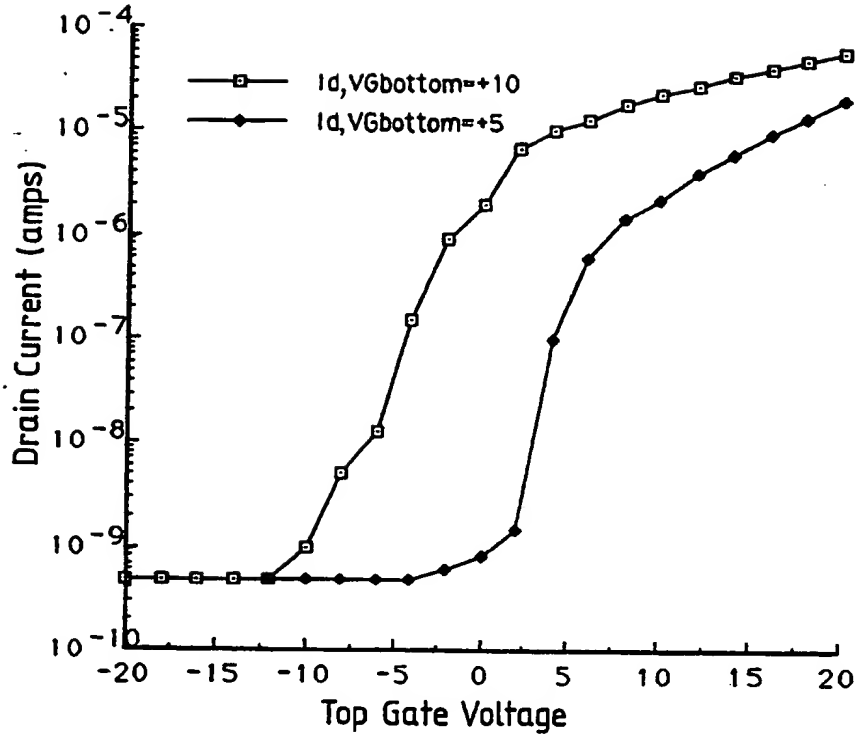

Id,VGbottom=+10
Id,VGbottom=+5
Drain Current (amps)
10^-4
10^-5
10^-6
10^-7
10^-8
10^-9
10^-10
-20
-15
-10
-5
0
5
10
15
20
Top Gate Voltage

Fig. 2

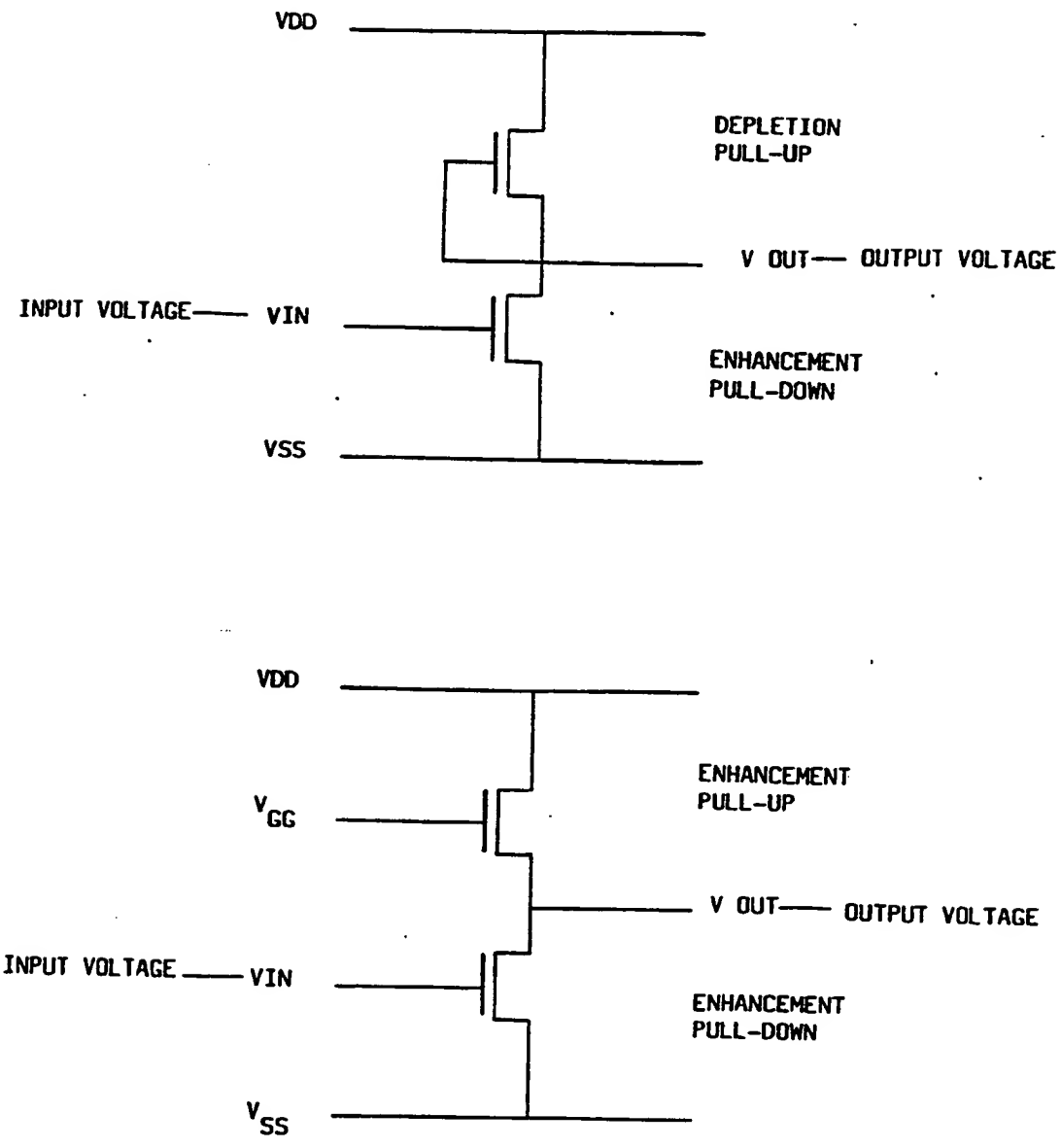

VDD
DEPLETION
PULL-UP
V OUT— OUTPUT VOLTAGE
INPUT VOLTAGE— VIN
ENHANCEMENT
PULL-DOWN
VSS
VDD
ENHANCEMENT
PULL-UP
$V_{GG}$
V OUT— OUTPUT VOLTAGE
INPUT VOLTAGE — VIN
ENHANCEMENT
PULL-DOWN
$V_{SS}$

Fig. 3

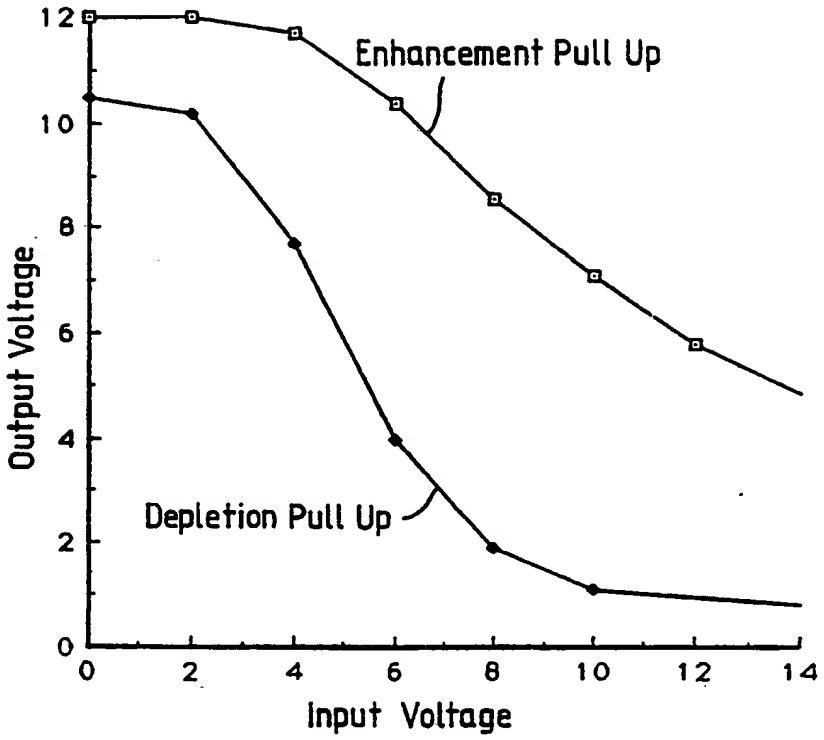

12
10
8
6
4
2
0
Output Voltage
Enhancement Pull Up
Depletion Pull Up
0
2
4
6
8
10
12
14
Input Voltage

Fig.4

# INTERNATIONAL SEARCH REPORT

International Application No PCT/GB 93/00792

## I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all)[6]

According to International Patent Classification (IPC) or to both National Classification and IPC

Int.Cl. 5 H01L29/784; H01L27/088

## II. FIELDS SEARCHED

Minimum Documentation Searched[7]

| Classification System | Classification Symbols |
|---|---|
| Int.Cl. 5 | H01L |

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched[8]

## III. DOCUMENTS CONSIDERED TO BE RELEVANT[9]

| Category ° | Citation of Document, [11] with indication, where appropriate, of the relevant passages [12] | Relevant to Claim No.[13] |
|---|---|---|
| X | PATENT ABSTRACTS OF JAPAN<br>vol. 007, no. 021 (E-155)27 January 1983<br>& JP,A,57 180 177 ( TOKYO SHIBAURA DENKI KK ) 6 November 1982<br>see abstract | 1 |
| Y | --- | 2,4,5 |
| Y | IBM TECHNICAL DISCLOSURE BULLETIN<br>vol. 20, no. 12, May 1978, NEW YORK US<br>page 5352<br>F. F. FANG 'TFT STRUCTURE WITH ELECTRONICALLY ADJUSTABLE THRESHOLD' | 2,4,5 |
| X | --- | 1,4,5 |
| | US,A,4 803 530 (TAGUCHI)<br>7 February 1989<br>see column 9, line 25 - column 10, line 16; figure 6 | |
| | --- | |
| | -/-- | |

° Special categories of cited documents : [10]

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

## IV. CERTIFICATION

| Date of the Actual Completion of the International Search | Date of Mailing of this International Search Report |
|---|---|
| 22 JUNE 1993 | 02. 07. 93 |
| **International Searching Authority** | **Signature of Authorized Officer** |
| EUROPEAN PATENT OFFICE | MIMOUN B.J. |

Form PCT/ISA/210 (second sheet) (January 1985)

III. DOCUMENTS CONSIDERED TO BE RELEVANT (CONTINUED FROM THE SECOND SHEET)

| Category ° | Citation of Document, with indication, where appropriate, of the relevant passages | Relevant to Claim No. |
|---|---|---|
| A | PATENT ABSTRACTS OF JAPAN<br>vol. 015, no. 229 (E-1076)11 June 1991<br>& JP,A,30 66 159 ( MITSUBISHI ELECTRIC CORP ) 20 March 1991<br>see abstract | 1,2,4,5 |
| A | IEEE ELECTRON DEVICE LETTERS<br>vol. 13, no. 1, January 1992, NEW YORK US<br>pages 17 - 19<br>BIING-SENG WU ET AL 'A Novel Depletion-Gate Amorphous Silicon Thin-Film Transistor'<br>see the whole document | 2,4,5 |
| A | EP,A,0 006 001 (THE SECRETARY OF STATE DEFENCE IN HER BRITANIC MAJ. GOV.)<br>12 December 1979<br>see page 15, line 13 - line 22 | 2 |
| A | EP,A,0 308 128 (NATIONAL RESEARCH DEVELOPMENT CORPORATION)<br>22 March 1989<br>see column 2, line 38 - column 3, line 28 | 2,3 |
| A | WO,A,9 006 595 (HUGHES AIRCRAFT COMPANY)<br>14 June 1990<br>see abstract; figure 1 | 2 |

# ANNEX TO THE INTERNATIONAL SEARCH REPORT ON INTERNATIONAL PATENT APPLICATION NO.

GB 9300792
SA 73120

This annex lists the patent family members relating to the patent documents cited in the above-mentioned international search report.
The members are as contained in the European Patent Office EDP file on
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information. 22/06/93

| Patent document cited in search report | Publication date | Patent family member(s) | Publication date |
|---|---|---|---|
| US-A-4803530 | 07-02-89 | JP-A- 54033679 | 12-03-79 |
| EP-A-0006001 | 12-12-79 | GB-A- 1601059 | 21-10-81 |
| | | AU-A- 4758379 | 06-12-79 |
| | | FR-A- 2427685 | 28-12-79 |
| | | JP-A- 54158881 | 15-12-79 |
| | | US-A- 4317125 | 23-02-82 |
| EP-A-0308128 | 22-03-89 | GB-A,B 2209870 | 24-05-89 |
| | | JP-A- 1152763 | 15-06-89 |
| | | US-A- 4968638 | 06-11-90 |
| WO-A-9006595 | 14-06-90 | EP-A- 0401356 | 12-12-90 |
| | | JP-T- 3503227 | 18-07-91 |